Amendments to the Specification:

Please replace the title with the following amended title:

MULTILAYER CIRCUIT

Please replace paragraph [0032] of the published application with the following amended paragraph:

[0032] Processing begins as shown in FIG. 3 by forming the intended conductor pattern into [[to]] two conductor layers 2 and 4 so that the conductor is alternately removed from the bottom and top sides of the insulator 3 from each segment. Generally speaking, this occurs at least from the places where connections between conductor layers will later be formed. The intention of the figures here is only to illustrate the manufacturing method, and the details of the conductor patterns are not considered. The removal of the conductor in places 2 and 4 reveals the insulating layer 3 where apertures 6 can be made into the insulator 3 according to FIG. 4. Apertures 6 can be formed for example by mechanical drilling, with laser or by etching with plasma or suitable chemical etching bath. It is also possible to pattern conductor layers 2 and 4 in multiple steps and for example to use conductor layers 2 and 4 as etching masks when apertures 6 are formed into insulator 3. The insulator 3 can also be etched in multiple steps. Other electronics manufacturing methods, such as additive conductor build up, photo-definable insulation; mechanical forming and lamination methods can also be used. Various different insulator, conductor and solder materials can also be used in manufacturing.

Please replace paragraph [0035] of the published application with the following amended paragraph:

[0035] The winding layers on top of each other are seen individually through the apertures 15, and the winding layers 13 can be contacted together for example with a rivet 16 which punches the conductors at the apertures according to FIG. 9. The rivet is formed to provide soldering possibility to a printed circuit board as well.

Please replace paragraph [0047] of the published application with the following amended paragraph:

[0047] In order to connect the finished multilayer structure 24 to the circuit board as a surface mounted component, it can be provided with a solder extension 23 which is then folded under the component to position 25 according to FIGS. 12A, 12B and 12C. Some layers of the structure can also be provided with mechanical dimples 28 or connection terminals 26 or interconnection balls 29 to provide electrical and mechanical contact to the substrate, as illustrated in FIG. 13. A conductor pattern on the outermost surface may also be used as sufficient interconnection surface. Connection extensions 23 can be used to provide both internal and external connections to the multilayer structure.